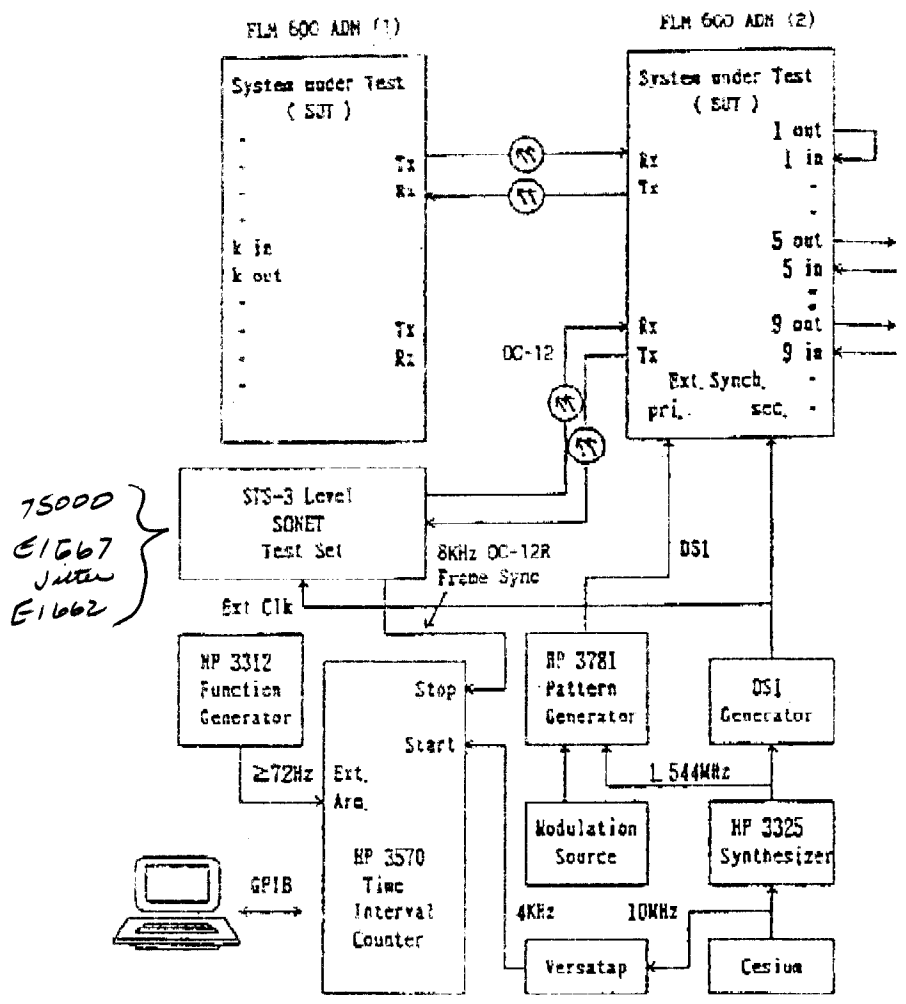


5.13.5 MTIE test (TCA-ENH)

5.13.5.1 OC-N

1) Test setup



75000
E1667
Jitter
E1662

Figure 5.13.5.1 Synchronization test setup

MTIE: This is usually pronounced "em tai". MTIE stands for maximum time interval error.

The master clock used by equipment such as ADM and LTE which conforms to SONET may shift its phase. MTIE is the amount by which this phase shifts over a given period. If this amount is excessive, pointer action frequently occurs with adverse effects in a synchronized network.

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2) Test procedure

- (1) Set a DSI signal that has 1 μ s of white noise jitter and is limited to the band between 10 and 150 Hz to BITS. Then, check that MTIE satisfies the specifications shown in Figure 5.13.5.2.
- (2) Operate the FLM 600 ADM2 on a line timing signal using OC-12 without jitter and wander as the source clock. Then, check that MTIE satisfies the specifications shown in Figure 5.13.5.2.
- (3) Operate the FLM 600 ADM2 on a line timing signal based on an OC-12 source clock having 1.5 UI or less of jitter after the 500-Hz-to-1.3-MHz bandpass filter or 0.15 UI or less of jitter after the 65-kHz-to-1.3-MHz bandpass filter. Then, check that MTIE satisfies the specifications shown in Figure 5.13.5.2.
- (4) Perform the operations described below, and check that TIE is 20 ns or less and MTIE is 1 μ s or less in any measurement interval of 14 ms or more. Perform these operations under each of the conditions described in (1) to (3) above.
 - Manual timing reference switching (primary <--> secondary)
 - Automatic timing reference switching (primary --> secondary due to failure)
 - Hold-over, or switching to internal clock or switching back from internal clock (recovery)
 - Phase shift of external synchronous input with the change rate specified in TI.101
 - Unit switching (for reference)

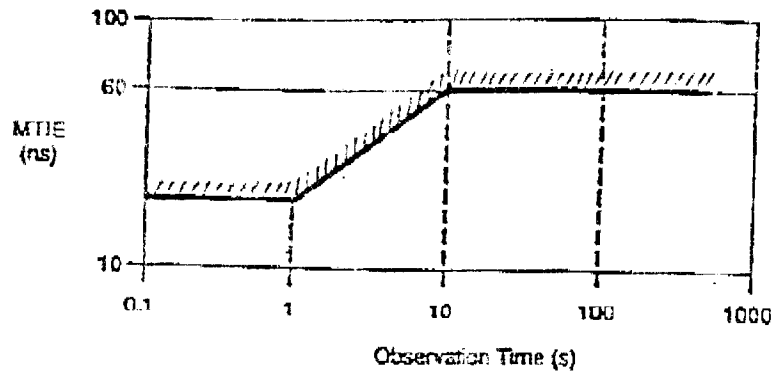


Figure 5.13.5.2 MTIE for SONET clocks

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